Testing (and defining) Weak Memory Models
A simple shared memory computer

Threads execute programs as usual: instructions are executed completely and atomically (memory stores in particular).
The Sequentially Consistent Model (SC)

Definition by L. Lamport:

"\ldots the result of any execution is the same as if the operations of all the processors were executed in some sequential order, and the operations of each individual processor appear in this sequence in the order specified by its program".

(One may add "stores take effect immediately").

**Interleaving semantics:** This is "interleaving semantics" as "some sequential order" results from interleaving "the order specified by the program of all individual processors".

A first, one expect shared memory multiprocessors to behave that way, which of course they don’t.
Axiomatic or *post-mortem* semantics — Events

The effects of “operations executed by the processors” are represented by events. We define *memory events* \( (a):d[\ell]v:\)

- Unique label typically \((a), (b), \text{etc.}\)
- Direction \(d\), that is read (R) or write (W)
- Memory location \(\ell\), typically \(x, y, \text{etc.}\)
- Value \(v\), typically \(0, 1, \text{etc.}\)
- Originating thread: \(T_0, T_1\) (often omitted)

The program order \(\xrightarrow{\text{po}}\) (“order specified by program”) is a linear order amongst the events originating from the same thread.

Relation \(\xrightarrow{\text{po}}\) represents the sequential execution of events by one thread that follows the *uniprocessor model*: the usual processor execution model, where instructions are executed by following the order given in program.
Example of program order

Despite its name, program order is a dynamic notion.

/* x, t and y are (shared) memory locations, t = { 2, 3, } */
int r1,r2=0 ; // non-shared locations (e.g. registers)
x = 1 ;
for (int k = 0 ; k < 2 ; k++) { r1 = t[k] ; r2 += r1 ; }  
y = r2 ;

Events and program order :

(a):W[x]1 \xrightarrow{PO} (b):R[t + 0]2 \xrightarrow{PO} (c):R[t + 4]3 \xrightarrow{PO} (d):W[y]5

Notice:  program order (and events) may depend on the values of the
reads, i.e. on values written by other threads (if . . . ).
In simple examples, program order is given by program text.
Relating writes and reads

We define a first “communication relation” between events with the same location.

**Definition (Read-from $\xrightarrow{\text{rf}}$)**

Relates write events to read events that read the stored value (implicit initial writes).

1. **Existence and unicity:**
   \[ \forall r, \exists ! w, w \xrightarrow{\text{rf}} r \]

2. **Same location, same value:**
   \[ \text{loc}(w) = \text{loc}(r) \land \text{val}(w) = \text{val}(r). \]
Example of $\mathbf{rf}\rightarrow$

\begin{center}
\begin{tabular}{|c|c|}
\hline
& \text{LB} \\
\hline
$T_0$ & $T_1$ \\
\hline
$(a) r_0 \leftarrow x$ & $(c) r_1 \leftarrow y$ \\
$(b) y \leftarrow 1$ & $(d) x \leftarrow 1$ \\
\hline
\end{tabular}
\end{center}

Observe: $r_0; r_1$;

(Intial values of \(x\) and \(y\) are 0.)

\begin{align*}
\text{r0=1; r1=1;} & \quad \text{r0=1; r1=0;} \\
\text{r0=0; r1=1;} & \quad \text{r0=0; r1=0;} \\
\end{align*}
Example of $\text{rf} \rightarrow$ LB

<table>
<thead>
<tr>
<th></th>
<th>$T_0$</th>
<th>$T_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>$r_0 \leftarrow x$</td>
<td>(c) $r_1 \leftarrow y$</td>
</tr>
<tr>
<td>(b)</td>
<td>$y \leftarrow 1$</td>
<td>(d) $x \leftarrow 1$</td>
</tr>
</tbody>
</table>

Observe: $r_0; r_1$;

(Initial values of $x$ and $y$ are 0.)

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$r_0=1; r_1=1;$</td>
<td>$r_0=1; r_1=0;$</td>
<td></td>
</tr>
<tr>
<td>a: $R_x=1$</td>
<td>c: $R_y=1$</td>
<td></td>
</tr>
<tr>
<td>b: $W_y=1$</td>
<td>d: $W_x=1$</td>
<td></td>
</tr>
<tr>
<td>po</td>
<td>po</td>
<td></td>
</tr>
<tr>
<td>r0=0; r1=1;</td>
<td>r0=0; r1=0;</td>
<td></td>
</tr>
</tbody>
</table>
Example of \( \rightarrow \)

<table>
<thead>
<tr>
<th>(T_0)</th>
<th>(T_1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) (r_0 \leftarrow x)</td>
<td>(c) (r_1 \leftarrow y)</td>
</tr>
<tr>
<td>(b) (y \leftarrow 1)</td>
<td>(d) (x \leftarrow 1)</td>
</tr>
</tbody>
</table>

Observe: \(r_0; r_1;\)

(Initial values of \(x\) and \(y\) are 0.)

\[
\begin{align*}
\text{a: } & R_x=1 & \text{c: } & R_y=1 \\
\text{b: } & W_y=1 & \text{d: } & W_x=1 \\
\text{r}_0=0; & \text{r}_1=1; & \text{r}_0=0; & \text{r}_1=0;
\end{align*}
\]
Example of $\rightarrow$ rf

<p>| | |</p>
<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>$T_0$</td>
<td>$T_1$</td>
</tr>
<tr>
<td>(a) $r_0 \leftarrow x$</td>
<td>(c) $r_1 \leftarrow y$</td>
</tr>
<tr>
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Observe: $r_0$; $r_1$;

(Intial values of $x$ and $y$ are 0.)

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<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$r_0=1$; $r_1=1$;</td>
<td>$r_0=1$; $r_1=0$;</td>
</tr>
</tbody>
</table>
| a: $R_x=1$ | c: $R_y=1$
| po $\rightarrow$ rf rf po |
| b: $W_y=1$ | d: $W_x=1$
| a: $R_x=1$ | c: $R_y=0$
| po $\rightarrow$ rf po |
| b: $W_y=1$ | d: $W_x=1$
| $r_0=0$; $r_1=1$; | $r_0=0$; $r_1=0$; |
Example of $rf \rightarrow$ LB

<table>
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<th>$T_0$</th>
<th>$T_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>$r_0 \leftarrow x$</td>
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<tr>
<td>(b)</td>
<td>$y \leftarrow 1$</td>
<td>$d) x \leftarrow 1$</td>
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</table>

Observe: $r_0; r_1$

(Intial values of $x$ and $y$ are 0.)

<table>
<thead>
<tr>
<th></th>
<th>$r_0=1; r_1=1$;</th>
<th>$r_0=1; r_1=0$;</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>$Rx=1$; $rfa: Rx=0$</td>
<td>$a: Rx=1$</td>
</tr>
<tr>
<td>b</td>
<td>$Wy=1$</td>
<td>$b: Wy=1$</td>
</tr>
<tr>
<td>c</td>
<td>$Ry=1$; $r: Ry=1$</td>
<td>$c: Ry=1$</td>
</tr>
<tr>
<td>d</td>
<td>$Wx=1$</td>
<td>$d: Wx=1$</td>
</tr>
</tbody>
</table>
Example of $\rightarrow_{rf}$

<table>
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<tr>
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Observe: $r_0; r_1$;

(Intial values of $x$ and $y$ are 0.)

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</tr>
</thead>
<tbody>
<tr>
<td>a:</td>
<td>$R_x=1$</td>
<td>$R_x=1$</td>
</tr>
<tr>
<td>b:</td>
<td>$W_y=1$</td>
<td>$W_y=1$</td>
</tr>
<tr>
<td>c:</td>
<td>$R_y=1$</td>
<td>$R_y=0$</td>
</tr>
<tr>
<td>d:</td>
<td>$W_x=1$</td>
<td>$W_x=1$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
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<th>$r_0=0; r_1=1$</th>
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<tbody>
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<tr>
<td>b:</td>
<td>$W_y=1$</td>
<td>$W_y=1$</td>
</tr>
<tr>
<td>c:</td>
<td>$R_y=1$</td>
<td>$R_y=0$</td>
</tr>
<tr>
<td>d:</td>
<td>$W_x=1$</td>
<td>$W_x=1$</td>
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</tbody>
</table>
A definition of SC

Definition (SC 1)

An execution is SC when there exists a total order on events <, such that:

1. Order < is compatible with program order:

   \[ e_1 \xrightarrow{\text{po}} e_2 \implies e_1 < e_2. \]

2. A Read \( r \) reads from the recent write before \( r \) in <.

\[
\xrightarrow{rf<} \quad \text{Def} \quad \left\{ (w, r) | w = \max(w', \text{loc}(w')) = \text{loc}(r) \land w' < r \right\}.
\]
A question on SC

Program:

<table>
<thead>
<tr>
<th></th>
<th>$T_0$</th>
<th>$T_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>$x \leftarrow 1$</td>
<td>(c) $y \leftarrow 2$</td>
</tr>
<tr>
<td>(b)</td>
<td>$y \leftarrow 1$</td>
<td>(d) $r_0 \leftarrow x$</td>
</tr>
</tbody>
</table>

Observed? $y=2$; $r_0=0$

How can we know? Let us enumerate all interleavings.

$a, b, c, d$
A question on SC

Program:

<table>
<thead>
<tr>
<th></th>
<th>$T_0$</th>
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<tbody>
<tr>
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Observed? $y=2$; $r0=0$

How can we know? Let us enumerate all interleavings.

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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$a, b, c, d$</td>
<td>$y=2; r0=1$</td>
<td></td>
</tr>
<tr>
<td>$a, c, b, d$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
A question on SC

Program:

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<tr>
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<th>$T_0$</th>
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</tr>
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<tbody>
<tr>
<td>(a)</td>
<td>$x \leftarrow 1$</td>
<td></td>
</tr>
<tr>
<td>(b)</td>
<td>$y \leftarrow 1$</td>
<td>$y \leftarrow 2$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(d) $r0 \leftarrow x$</td>
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</table>

Observed? $y=2$; $r0=0$

How can we know? Let us enumerate all interleavings.

- $a, b, c, d$  \quad y=2; r0=1;
- $a, c, b, d$  \quad y=1; r0=1;
- $a, c, d, b$  \quad
A question on SC

Program:

<table>
<thead>
<tr>
<th>R</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$T_0$</td>
</tr>
<tr>
<td></td>
<td>$T_1$</td>
</tr>
<tr>
<td>(a) $x \leftarrow 1$</td>
<td>(c) $y \leftarrow 2$</td>
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<td>Observed? $y=2$; $r0=0$</td>
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How can we know? Let us enumerate all interleavings.

<table>
<thead>
<tr>
<th>$a, b, c, d$</th>
<th>$y=2; r0=1$;</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a, c, b, d$</td>
<td>$y=1; r0=1$;</td>
</tr>
<tr>
<td>$a, c, d, b$</td>
<td>$y=1; r0=1$;</td>
</tr>
<tr>
<td>$c, d, a, b$</td>
<td></td>
</tr>
</tbody>
</table>
A question on SC

Program:

<table>
<thead>
<tr>
<th></th>
<th>$T_0$</th>
<th>$T_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(a)$</td>
<td>$x \leftarrow 1$</td>
<td>$(c) \ y \leftarrow 2$</td>
</tr>
<tr>
<td>$(b)$</td>
<td>$y \leftarrow 1$</td>
<td>$(d) \ r0 \leftarrow x$</td>
</tr>
</tbody>
</table>

Observed? $y=2; \ r0=0$

How can we know? Let us enumerate all interleavings.

- $a, b, c, d$ \hspace{3cm} $y=2; \ r0=1$
- $a, c, b, d$ \hspace{3cm} $y=1; \ r0=1$
- $a, c, d, b$ \hspace{3cm} $y=1; \ r0=1$
- $c, d, a, b$ \hspace{3cm} $y=1; \ r0=0$
- $c, a, b, d$ \hspace{3cm} $y=1; \ r0=0$

Conclusion: No SC execution would ever yield the output "$y=2; \ r0=0$".
A question on SC

Program:

<table>
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<tr>
<th></th>
<th>$T_0$</th>
<th>$T_1$</th>
</tr>
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<tbody>
<tr>
<td>(a)</td>
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<td>(c)</td>
</tr>
<tr>
<td>(b)</td>
<td>$y \leftarrow 1$</td>
<td>(d)</td>
</tr>
</tbody>
</table>

Observed? $y=2; r_0=0$

How can we know? Let us enumerate all interleavings.

- $a, b, c, d$, $y=2; r_0=1$
- $a, c, b, d$, $y=1; r_0=1$
- $a, c, d, b$, $y=1; r_0=1$
- $c, d, a, b$, $y=1; r_0=0$
- $c, a, b, d$, $y=1; r_0=1$
- $c, a, d, b$
A question on SC

Program:

<table>
<thead>
<tr>
<th></th>
<th>T₀</th>
<th>T₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>x ← 1</td>
<td>(c)</td>
</tr>
<tr>
<td>(b)</td>
<td>y ← 1</td>
<td>(d)</td>
</tr>
</tbody>
</table>

Observed? y=2; r₀=0

How can we know? Let us enumerate all interleavings.

<table>
<thead>
<tr>
<th></th>
<th>y=2; r₀=1;</th>
</tr>
</thead>
<tbody>
<tr>
<td>a, b, c, d</td>
<td></td>
</tr>
<tr>
<td>a, c, b, d</td>
<td></td>
</tr>
<tr>
<td>a, c, d, b</td>
<td></td>
</tr>
<tr>
<td>c, d, a, b</td>
<td></td>
</tr>
<tr>
<td>c, a, b, d</td>
<td></td>
</tr>
<tr>
<td>c, a, d, b</td>
<td></td>
</tr>
</tbody>
</table>

Conclusion: No SC execution would ever yield the output “y=2; r₀=0;”.
Modern machines are not SC, how can we know?

```c
void *T0(void *p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    q->x = 1;
    q->y = 1;
    return NULL;
}
```

```c
void *T1(void *p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    q->y = 2;
    int r0 = q->x;
    q->r0 = r0;
    return NULL;
}
```
Modern machines are not SC, how can we know?

```c
void *T0(void *p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    q->x = 1;
    q->y = 1;
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void *T1(void *p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    q->y = 2;
    int r0 = q->x;
    q->r0 = r0;
    return NULL;
}

for (; ;) {
    // Initialise
    common_t c; c.x = c.y = 0; ctx_t a0,a1;
    // Run
    a0.id = 0; a0.common = &c; create_thread(&th0,T0,&a0);
    a1.id = 1; a1.common = &c; create_thread(&th1,T1,&a1);
    join_thread(&th0);
    join_thread(&th1);
    // Collect results
    ... c.y ... c.r0
}
```
Naive testing, graphically

Let us run test $R$ on this machine (demo/01/naive_r.out)
Minimizing the impact of thread creation on cost

We perform size tests per thread creation, in arrays.

```c
void *T0(void *p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    for (int k = 0; k < q->size; k++) {
        q->x[k] = 1;
        q->y[k] = 1;
    }
    return NULL;
}
```

```c
void *T1(void *p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    for (int k = 0; k < q->size; k++) {
        q->y[k] = 2;
        int r0 = q->x[k];
        q->r0[k] = r0;
    }
    return NULL;
}
```
Graphically

Let us run test $R$ on this machine (demo/01/loop_r.out)
Let us synchronise iterations

```c
void *T0(void *_p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    for (int k = 0; k < q->size; k++) {
        wait_partner(&q->sync[k], k, 0);
        q->x[k] = 1;
        q->y[k] = 1;
    }
    return NULL;
}

void *T1(void *_p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    for (int k = 0; k < q->size; k++) {
        wait_partner(&q->sync[k], k, 1);
        q->y[k] = 2;
        int r0 = q->x[k];
        q->r0[k] = r0;
    }
    return NULL;
}
```

Let us synchronise iterations

```c
void *T0(void *p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    for (int k = 0; k < q->size; k++) {
        wait_partner(&q->sync[k], k, 0);
        q->x[k] = 1;
        q->y[k] = 1;
    }
    return NULL;
}

void *T1(void *p) {
    ctx_t *p = _p;
    common_t *q = p->common;
    for (int k = 0; k < q->size; k++) {
        wait_partner(&q->sync[k], k, 1);
        q->y[k] = 2;
        int r0 = q->x[k];
        q->r0[k] = r0;
    }
    return NULL;
}

inline static void wait_partner(volatile int *p, int k, int id) {
    if (k % 2 == id) {
        *p = 1; __sync_synchronize(); // Well...
    } else {
        while (*p == 0);
    }
}
```
Let us run test R on this machine (demo/01-sync_r.out)
Running $n$ test instances at once

Why not run $n = \lfloor a/2 \rfloor$ instances of $R$ on a $a$-core machine?

- Much more outcomes on many-core machines per test run
- Important when one pays resources by chunks of say 32 cores.
- Makes noise and favors outcome variability.
The litmus tool

Tests are written in assembler, for precision.

X86 R
{ }  
P0     | P1     ;
MOV [x],$1 | MOV [y],$2  ;
MOV [y],$1 | MOV EAX,[x]  ;
exists (y=2 \ 1:EAX=0)

Tests are compiled to C programs (with inline assembler):

```
file.litmus
```
```
litmus
```
```
file.c
```
```
gcc -pthread
```
```
file.exe
```

Demo in demo/02:

```
% litmus -mach ./x86.cfg -o run R.litmus
% cd run
% make
% ./R.exe -v -v
```
Some litmus settings

- Synchronisation
  - Loose synchronisation (we saw it).
  - Exact synchronisation with polling synchronisation barriers and time base.
  - Other, less useful, modes: POSIX thread barrier based and no synchronisation at all.

- Affinity: force threads to run on designated cores, or let the OS scheduler perform its job.

- Prefetching of flushing cache lines.
  - Automatic, depending on test.
  - Random.
  - Complete or none.

- Various scanning order of location arrays.
  - Random (by the means of a shuffled array of pointer).
  - Linear with a stride.

A complete testing campaign usually involves trying many settings (for instance, testing all strides from 1 to cache line size).
Perfect! We know how to run tests on hardware, but
Building significant tests

Perfect! We know how to run tests on hardware, but what tests do we run?

We study *relaxed* memory models, that is *relaxed* w.r.t SC.

Hence, we focus on programs that have non-SC behaviours.

The question is: how do we generate such programs.

Let us study SC in detail first.
Back to our non-SC example

<table>
<thead>
<tr>
<th>T₀</th>
<th>T₁</th>
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<tbody>
<tr>
<td>(a) x ← 1</td>
<td>(c) y ← 2</td>
</tr>
<tr>
<td>(b) y ← 1</td>
<td>(d) r₀ ← x</td>
</tr>
</tbody>
</table>

Observed? y=2; r₀=0

All interleavings.

| a, b, c, d | y=2; r₀=1; |
| a, c, b, d | y=1; r₀=1; |
| a, c, d, b | y=1; r₀=1; |
| c, d, a, b | y=1; r₀=0; |
| c, a, b, d | y=1; r₀=1; |
| c, a, d, b | y=1; r₀=1; |

We observe if b < c then y=2, if d < a then r₀=0.
Let us be a bit more clever

<table>
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<td>(b) $y \leftarrow 1$</td>
<td>(d) $r0 \leftarrow x$</td>
<td></td>
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Observed? $y=2; \ r0=0$

Collecting constraints on the scheduling order $<$:

We respect program order, thus
Let us be a bit more clever

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Observed? $y=2$; $r0=0$

Collecting constraints on the scheduling order $<$:

We respect program order, thus $a < b$ and $c < d$. We observe $r0=0$, thus
Let us be a bit more clever

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Observed? $y=2$; $r_0=0$

Collecting constraints on the scheduling order $<$:

We respect program order, thus $a < b$ and $c < d$.
We observe $r_0=0$, thus $d < a$.
We observe $y=2$, thus
Let us be a bit more clever

\[
\begin{array}{c|c}
R & \\
\hline
T_0 & T_1 \\
\hline
(a) x & (c) y \\
\hline
(b) y & (d) r0 \\
\end{array}
\]

Observed? y=2; r0=0

Collecting constraints on the scheduling order <:

We respect program order, thus \( a < b \) and \( c < d \).
We observe \( r0=0 \), thus \( d < a \).
We observe \( y=2 \), thus \( b < c \).

Hence we have a cycle in <, which prevents it from being an order!

\[a < b < c < d < a \ldots\]

**Conclusion:** No SC execution would ever yield the output “y=2; r0=0;”.
Systematic approach

For a particular (partial) execution candidate (that is, for a set of events and a $\rightarrow^{po}$ relation) we assume two additional relations:

- **Read-from ($\rightarrow^{rf}$):** Relates write events to read events that read the stored value (implicit initial writes).
  
  $\forall r, \exists! w, w \rightarrow^{rf} r$

- **Coherence ($\rightarrow^{co}$):** Relates write events to the same location.
  
  For any location $\ell$, the restriction of $\rightarrow^{co}$ to write events to location $\ell (W_\ell)$ is a total order.

**Notice:** To me, the very existence of $\rightarrow^{co}$ stems from the existence of a shared, coherent, memory — Given location $\ell$, there is exactly one memory cell whose location is $\ell$. 
Example of $\longrightarrow$ 2+2W

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Observe: $x; y$

---

$x=1; y=2;$

$x=1; y=1;$

$x=2; y=2;$

$x=2; y=1;$
Example of $\xrightarrow{\text{co}}$

$$2 + 2W$$

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Observe: $x; y$;

<p>| | | |</p>
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<td>$x=1; y=2;$</td>
<td></td>
<td>$x=1; y=1;$</td>
</tr>
</tbody>
</table>

- **a**: $Wx=2$
- **b**: $Wy=1$
- **c**: $Wy=2$
- **d**: $Wx=1$

<p>| | | |</p>
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<thead>
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<tr>
<td>$x=2; y=2;$</td>
<td></td>
<td>$x=2; y=1;$</td>
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<p>| | | |</p>
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<tr>
<td></td>
<td>$\text{p}o$</td>
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$\text{p}o$
Example of $\text{co}$

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Observe: $x; y$

---

$x=1; y=2$

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<th>$Wy=2$</th>
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<tbody>
<tr>
<td>a:</td>
<td>$\text{po}$</td>
<td>$\text{co}$</td>
</tr>
<tr>
<td>b:</td>
<td>$Wy=1$</td>
<td>$Wx=1$</td>
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$x=1; y=1$

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---

$x=2; y=2$

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<tr>
<td>d:</td>
<td>$\text{po}$</td>
<td>$\text{co}$</td>
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$x=2; y=1$

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Example of $\rightarrow^\text{co}$

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Observe: $x; y$;

---

$x=1;\ y=2;$

- $a$: $Wx=2$
- $b$: $Wy=1$
- $c$: $Wx=1$
- $d$: $Wy=2$

---

$x=1;\ y=1;$

- $a$: $Wx=2$
- $b$: $Wy=1$
- $c$: $Wx=1$
- $d$: $Wy=2$

---

$x=2;\ y=2;$

- $a$: $Wx=2$
- $b$: $Wy=1$
- $c$: $Wx=1$
- $d$: $Wy=2$

---

$x=2;\ y=1;$

- $a$: $Wx=2$
- $b$: $Wy=1$
- $c$: $Wx=1$
- $d$: $Wy=2$
Example of $\rightarrow$

| $2+2W$ |
|---|---|
| $T_0$ | $T_1$ |
| (a) $x \leftarrow 1$ | (c) $y \leftarrow 1$ |
| (b) $y \leftarrow 2$ | (d) $x \leftarrow 2$ |

Observe: $x$; $y$;

$x=1$; $y=2$;

a: $Wx=2$  c: $Wy=2$

\[
\begin{array}{c}
\text{po} \\
\text{CO}
\end{array}
\quad
\begin{array}{c}
\text{po} \\
\text{CO}
\end{array}
\]

b: $Wy=1$  d: $Wx=1$

$x=1$; $y=1$;

a: $Wx=2$  c: $Wy=2$

\[
\begin{array}{c}
\text{po} \\
\text{CO}
\end{array}
\quad
\begin{array}{c}
\text{po} \\
\text{CO}
\end{array}
\]

b: $Wy=1$  d: $Wx=1$

$x=2$; $y=2$;

a: $Wx=2$  c: $Wy=2$

\[
\begin{array}{c}
\text{po} \\
\text{COCO}
\end{array}
\quad
\begin{array}{c}
\text{po} \\
\text{COCO}
\end{array}
\]

b: $Wy=1$  d: $Wx=1$

$x=2$; $y=1$;

a: $Wx=2$  c: $Wy=2$

\[
\begin{array}{c}
\text{po} \\
\text{CO}
\end{array}
\quad
\begin{array}{c}
\text{po} \\
\text{CO}
\end{array}
\]

b: $Wy=1$  d: $Wx=1$
One more relation: \( \text{fr} \rightarrow \)

The new relation \( \text{fr} \rightarrow \) (from read) relates reads to "younger writes" (younger w.r.t. \( \text{co} \rightarrow \)).

\[
\begin{align*}
\text{Def} & \quad r \overset{\text{fr}}{\rightarrow} w \quad \text{Def} \quad w' \overset{\text{rf}}{\rightarrow} r \land w' \overset{\text{co}}{\rightarrow} w
\end{align*}
\]

This amounts to place a read into the coherence order of its location. Given

We have
One more relation: \( \text{fr} \rightarrow \)

The new relation \( \text{fr} \rightarrow \) (from read) relates reads to “younger writes” (younger w.r.t. \( \text{co} \rightarrow \)).

\[
  r \xrightarrow{\text{fr}} w \quad \text{Def} \quad w' \xrightarrow{\text{rf}} r \land w' \xrightarrow{\text{co}} w
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This amounts to place a read into the coherence order of its location. Given

We have
Particular, easy, case: a read from the initial state is in $\xrightarrow{\text{fr}}$ with writes by the program.

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Observed? $r_0=1$; $r_1=0$

a: $W_x=1$  c: $R_y=1$

b: $W_y=1$  d: $R_x=0$
Playing with \[\text{fr}\]

Particular, easy, case: a read from the initial state is in \[\text{fr}\] with writes by the program.

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<tr>
<td>(b) (y \leftarrow 1)</td>
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</table>

Observe? \(r0=1; r1=0\)

\[
\begin{array}{l}
\text{a: } Wx=1 \\
\text{b: } Wy=1 \\
\text{c: } Ry=1 \\
\text{d: } Rx=0
\end{array}
\]
Playing with $\rightarrow$ fr

Particular, easy, case: a read from the initial state is in $\rightarrow$ fr with writes by the program.

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Observed? $r_0=1; r_1=0$

a: $Wx=1$  c: $Ry=1$
b: $Wy=1$  d: $Rx=0$

Observed? $r_0=1; r_1=0$
Playing with \( \rightarrow \)

Particular, easy, case: a read from the initial state is in \( \rightarrow \) with writes by the program.

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<td>( b )</td>
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Observed? \( r_0=1; r_1=0 \)

- a: \( W_x=1 \)
- b: \( W_y=1 \)
- c: \( R_y=1 \)
- d: \( R_x=0 \)
Playing with \( \rightarrow \)

Particular, easy, case: a read from the initial state is in \( \rightarrow \) with writes by the program.

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<tr>
<td>Observed?</td>
<td>( r₀=0; \ r₁=0 )</td>
<td></td>
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a: \( Wx=1 \)  
\( po \)  
\( \downarrow \)  
\( \text{frfrf} \)  
b: \( Wy=1 \)  
\( \downarrow \)  
c: \( Ry=1 \)  
\( po \)  
d: \( Rx=0 \)  
\( \downarrow \)  

c: \( Wy=1 \)  
\( po \)  
\( \downarrow \)  
b: \( Ry=0 \)  
\( \downarrow \)  
d: \( Rx=0 \)  
\( \downarrow \)
Playing with $\xrightarrow{\text{fr}}$

Particular, easy, case: a read from the initial state is in $\xrightarrow{\text{fr}}$ with writes by the program.

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<td>(b)</td>
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<tr>
<td>Observed?</td>
<td>$r_0=1$; $r_1=0$</td>
<td>Observed?</td>
<td>$r_0=0$; $r_1=0$</td>
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Observations:

- **a:** $Wx=1$
- **b:** $Wy=1$
- **c:** $Ry=1$
- **d:** $Rx=0$
Playing with \(\rightarrow\)

Particular, easy, case: a read from the initial state is in \(\rightarrow\) with writes by the program.

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Observed? \(r_0=1; r_1=0\)

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Observed? \(r_0=0; r_1=0\)

\(a: Wx=1\) \(b: Wy=1\) \(c: Ry=1\) \(d: Rx=0\)

\(a: Wx=1\) \(b: Ry=0\) \(c: Wy=1\) \(d: Rx=0\)
Playing with $\rightarrow$

Particular, easy, case: a read from the initial state is in $\rightarrow$ with writes by the program.

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<td>$r_0=0$; $r_1=0$</td>
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a: $W_x=1$
po
b: $W_y=1$
fr
fr

b: $R_y=0$
fr
fr
d: $R_x=0$
po

a: $W_x=1$
po
c: $W_y=1$
po
d: $R_x=0$
Second definition of SC

Definition (SC 2)

An execution is SC when:

\[
\text{Acyclic}\left(\xrightarrow{\text{rf}} \cup \xrightarrow{\text{co}} \cup \xrightarrow{\text{fr}} \cup \xrightarrow{\text{po}}\right)
\]

And of course:
Second definition of SC

Definition (SC 2)

An execution is SC when:

$$\text{Acyclic} \left( \overset{\text{rf}}{\bigcup} \overset{\text{co}}{\bigcup} \overset{\text{fr}}{\bigcup} \overset{\text{po}}{\bigcup} \right)$$

And of course:

Theorem

*The two definitions of SC are equivalent.*
Introducing herd a memory model simulator

A model sc.cat:

% cat sc.cat
"Sequential consistency"
let com = rf | co | fr
acyclic (po | com) as hb

Running R on SC (demo in demo/02):

Test R Allowed
States 3
1:EAX=0; y=1;
1:EAX=1; y=1;
1:EAX=1; y=2;
No
Witnesses
Positive: 0 Negative: 3
Condition exists (y=2 \ 1:EAX=0)
Observation R Never 0 3

Notice: Outcome 1:EAX=0; y=2; is forbidden by SC.
Herd structure

- Generate all candidate executions, i.e. all possible $\rightarrow$, $\rightarrow$ and $\rightarrow$ ($\rightarrow$ deduced):

\[
\begin{align*}
\text{(a)}: & \quad W_x=1 \\
\text{(b)}: & \quad W_y=1 \\
\text{(c)}: & \quad W_y=2 \\
\text{(d)}: & \quad R_x=1
\end{align*}
\]
Herd structure

- Generate all candidate executions, i.e. all possible $\rightarrow_{po}$, $\rightarrow_{rf}$ and $\rightarrow_{co}$ ($\rightarrow_{fr}$ deduced):

  a: $Wx=1$
  b: $Wy=1$
  c: $Wy=2$
  d: $Rx=1$

  Ok

  a: $Wx=1$
  b: $Wy=1$
  c: $Wy=2$
  d: $Rx=0$

  No

- Apply model checks to each candidate execution.
Violations of SC

A cycle of $\rightarrow$, $\rightarrow$, $\rightarrow$, $\rightarrow$ describes a violation of SC.
From such a cycle, one may easily generate programs that potentially violate SC, and run them on an actual machine.

However, the cycle does not describe:

- How many threads are involved.
- How many memory locations are involved.

We now aim at:

- Extract a subset of *significant* cycles.
- Generate *one* program out of one cycle.
Simplifying cycles: \( \text{po} \rightarrow \) and \( \text{com} \rightarrow \) steps alternate

A cycle in \( \text{com} \rightarrow \cup \text{po} \rightarrow \) is a cycle in \( (\text{po}^{+}; \text{com}^{+}) \) (group \( \text{po} \rightarrow \) and \( \text{com} \rightarrow \) steps together). Then:

\begin{itemize}
  \item \( \text{po} \rightarrow \) is transitive \( \text{po}^{+} \subseteq \text{po} \).
  \item \( \text{com}^{+} \rightarrow \) is the union of the five following relations:

\[
\text{com}^{+} = \text{rf} \rightarrow \cup \text{co} \rightarrow \cup \text{fr} \rightarrow \cup
\]
\end{itemize}
Simplifying cycles: \( \text{po} \rightarrow \) and \( \text{com} \rightarrow \) steps alternate

A cycle in \( \text{com} \rightarrow \cup \text{po} \rightarrow \) is a cycle in \( (\text{po}^+; \text{com}^+) \) (group \( \text{po} \rightarrow \) and \( \text{com} \rightarrow \) steps together). Then:

- \( \text{po} \rightarrow \) is transitive \( \text{po}^+ \subseteq \text{po} \).
- \( \text{com}^+ \rightarrow \) is the union of the five following relations:

\[
\text{com} \rightarrow = \text{rf} \rightarrow \cup \text{co} \rightarrow \cup \text{fr} \rightarrow \cup \left( \text{co} \rightarrow ; \text{rf} \rightarrow \right) \cup
\]
Simplifying cycles: \( \overset{\text{po}}{\rightarrow} \) and \( \overset{\text{com}}{\rightarrow} \) steps alternate

A cycle in \( \overrightarrow{\text{com}} \cup \overrightarrow{\text{po}} \) is a cycle in \( (\overrightarrow{\text{po}}^+; \overrightarrow{\text{com}}^+) \) (group \( \overrightarrow{\text{po}} \) and \( \overrightarrow{\text{com}} \) steps together). Then:

- \( \overset{\text{po}}{\rightarrow} \) is transitive \( \overset{\text{po}}{\rightarrow}^+ \subseteq \overset{\text{po}}{\rightarrow} \).
- \( \overset{\text{com}}{\rightarrow}^+ \) is the union of the five following relations:

\[
\overrightarrow{\text{com}}^+ = \overrightarrow{\text{rf}} \cup \overrightarrow{\text{co}} \cup \overrightarrow{\text{fr}} \cup \left( \overrightarrow{\text{co}}; \overrightarrow{\text{rf}} \right) \cup \left( \overrightarrow{\text{fr}}; \overrightarrow{\text{rf}} \right).
\]

Because \( \left( \overrightarrow{\text{co}}; \overrightarrow{\text{co}} \right) \subseteq \overrightarrow{\text{co}} \), \( \left( \overrightarrow{\text{fr}}; \overrightarrow{\text{co}} \right) \subseteq \overrightarrow{\text{fr}} \), and \( \left( \overrightarrow{\text{fr}}; \overrightarrow{\text{fr}} \right) \subseteq \overrightarrow{\text{co}} \).

**Conclusion:** Any cyclic \( \overrightarrow{\text{com}} \cup \overrightarrow{\text{po}} \) includes a cycle in \( (\overrightarrow{\text{po}}; \overrightarrow{\text{com}}) \) — i.e. that alternates \( \overset{\text{po}}{\rightarrow} \) steps and \( \overset{\text{com}}{\rightarrow} \) steps.
Simplifying cycles: all $\xrightarrow{\text{com}}$ steps are external

Given a cycle, we consider all $\xrightarrow{\text{com}}$ and $\xrightarrow{\hat{\text{com}}}$ steps are external, that is source and target events are from pairwise distinct thread.

Given $e_1 \xrightarrow{\text{com}} e_2$, s.t. $e_1$ and $e_2$ are from the same thread:

- Either $e_1 \xrightarrow{\text{po}} e_2$ and we consider this $\xrightarrow{\text{po}}$ step in the cycle, in place of the $\xrightarrow{\text{com}}$ step.

- Or $e_2 \xrightarrow{\text{po}} e_1$ and we have a very simple cycle $e_2 \xrightarrow{\text{po}} e_1 \xrightarrow{\hat{\text{com}}} e_2$. Such cycles are “violations of coherence” (more on them later).

**Notice:** The same reasoning applies individual $\xrightarrow{\text{com}}$ steps in composite $\xrightarrow{\hat{\text{com}}}$.
Simplifying cycles — Locations

Cycle: \( W \xrightarrow{po} W \xrightarrow{rf} R \xrightarrow{po} R \xrightarrow{fr} W \xrightarrow{po} W \xrightarrow{rf} R \xrightarrow{po} R \xrightarrow{fr} \)

- One interpretation (four locations):
  a: \( Rx=1 \)  
  b: \( Wy=1 \)  
  c: \( Ry=1 \)  
  d: \( Wz=1 \)  
  e: \( Rz=1 \)  
  f: \( Wa=1 \)  
  g: \( Ra=1 \)  
  h: \( Wx=1 \) 

- Another interpretation (two locations):
  a: \( Rx=2 \)  
  b: \( Wy=1 \)  
  c: \( Ry=1 \)  
  d: \( Wx=1 \)  
  e: \( Rx=1 \)  
  f: \( Wy=2 \)  
  g: \( Ry=2 \)  
  h: \( Wx=2 \)
The second interpretation is not “minimal”

Reminding the interpretation with two locations:

\[
\begin{align*}
  &a: R_x=2 \quad c: R_y=1 \quad e: R_x=1 \quad g: R_y=2 \\
  &b: W_y=1 \quad d: W_x=1 \quad f: W_y=2 \quad h: W_x=2
\end{align*}
\]

But, coherence $\xrightarrow{\text{co}}$ totally orders write events to a given location.
The second interpretation is not “minimal”

Reminding the interpretation with two locations:

\[
\begin{align*}
 & a: Rx=2 \\
 & b: Wy=1 \\
 & c: Ry=1 \\
 & d: Wx=1 \\
 & e: Rx=1 \\
 & f: Wy=2 \\
 & g: Ry=2 \\
 & h: Wx=2
\end{align*}
\]

But, coherence $\rightarrow_{co}$ totally orders write events to a given location.

Let us choose: $Wx1 \rightarrow_{co} Wx2$:

\[
\begin{align*}
 & a: Rx=2 \\
 & b: Wy=1 \\
 & c: Ry=1 \\
 & d: Wx=1 \\
 & e: Rx=1 \\
 & f: Wy=2 \\
 & g: Ry=2 \\
 & h: Wx=2
\end{align*}
\]

We have a smaller cycle: $d \rightarrow_{co} h \rightarrow_{rf} a \rightarrow_{po} b \rightarrow_{rf} c \rightarrow_{po} d$. 
The second interpretation is not “minimal”

Reminding the interpretation with two locations:

\[
\begin{align*}
&\text{a: } Rx=2 & &\text{c: } Ry=1 & &\text{e: } Rx=1 & &\text{g: } Ry=2 \\
&\text{b: } Wy=1 & &\text{d: } Wx=1 & &\text{f: } Wy=2 & &\text{h: } Wx=2
\end{align*}
\]

But, coherence $\xrightarrow{co}$ totally orders write events to a given location.

Let us choose: $Wx2 \xrightarrow{co} Wx1$:

\[
\begin{align*}
&\text{a: } Rx=2 & &\text{c: } Ry=1 & &\text{e: } Rx=1 & &\text{g: } Ry=2 \\
&\text{b: } Wy=1 & &\text{d: } Wx=1 & &\text{f: } Wy=2 & &\text{h: } Wx=2
\end{align*}
\]

We have a smaller cycle: \( h \xrightarrow{co} d \xrightarrow{rf} e \xrightarrow{po} f \xrightarrow{rf} g \xrightarrow{po} h \).
The second interpretation is not “minimal”

Reminding the interpretation with two locations:

a: Rx=2
b: Wy=1

c: Ry=1
d: Wx=1

e: Rx=1
f: Wy=2
g: Ry=2
h: Wx=2

But, coherence $\xrightarrow{\co}$ totally orders write events to a given location.

Generally: do not repeat locations in cycles.
Simplifying cycles — Threads

Cycle: $W \xrightarrow{po} W \xrightarrow{rf} R \xrightarrow{po} R \xrightarrow{fr} W \xrightarrow{po} W \xrightarrow{rf} R \xrightarrow{po} R \xrightarrow{fr}$

- a: $Rx=1$
- b: $Wy=1$
- c: $Rz=1$
- d: $Wa=1$
- e: $Ry=1$
- f: $Wz=1$
- g: $Ra=1$
- h: $Wx=1$
Simplifying cycles — Threads

Cycle: \( W \xrightarrow{po} W \xrightarrow{rf} R \xrightarrow{po} R \xrightarrow{fr} W \xrightarrow{po} W \xrightarrow{rf} R \xrightarrow{po} R \xrightarrow{fr} \)

- a: \( Rx=1 \)
- b: \( Wy=1 \)
- c: \( Rz=1 \)
- d: \( Wa=1 \)
- e: \( Ry=1 \)
- f: \( Wz=1 \)
- g: \( Ra=1 \)
- h: \( Wx=1 \)
Simplifying cycles — Threads

Cycle: $W \xrightarrow{po} W \xrightarrow{rf} R \xrightarrow{po} R \xrightarrow{fr} W \xrightarrow{po} W \xrightarrow{rf} R \xrightarrow{po} R \xrightarrow{fr}$

a: $Rx=1$  e: $Ry=1$

b: $Wy=1$  f: $Wz=1$

c: $Rz=1$  g: $Ra=1$

d: $Wa=1$  h: $Wx=1$

Generally: one passage per thread
... Simplifying cycles

In a non SC execution we find:

- A *violation of coherence*, that is a cycle $e_1 \xrightarrow{po} e_2 \xrightarrow{com} e_1$.
- Or a *critical cycle* that is:
  - The cycle alternates $\xrightarrow{po}$ steps and external $\xrightarrow{com}$ steps, with at least four steps.
  - The cycle passes through a given thread at most once.
  - All $\xrightarrow{com}$ steps have pairwise different locations.
  - The source and target of one given $\xrightarrow{po}$ steps have different locations.

*Notice:* For a more formal presentation see D. Shasha and M. Snir Toplas 88 article, which introduced critical cycles.
Violations of coherence

There are five such cycles, which can occur as the following executions:

$$ po \rightarrow \text{contradicts} $$
Violations of coherence

There are five such cycles, which can occur as the following executions:
\[
\begin{align*}
\text{po} & \rightarrow \text{contradicts} \rightarrow \text{co}, \\
a: \ Wx=1 \\
b: \ Wx=2
\end{align*}
\]

CoWW
Violations of coherence

There are five such cycles, which can occur as the following executions:

\[\overset{\text{po}}{\rightarrow}\text{ contradicts }\overset{\text{co}}{\rightarrow},\overset{\text{rf}}{\rightarrow},\]

\(\begin{align*}
a: & \ Wx=1 \\
b: & \ Wx=2
\end{align*}\)

\(\begin{align*}
a: & \ Rx=1 \\
b: & \ Wx=1
\end{align*}\)

CoWW

CoRW1
Violations of coherence

There are five such cycles, which can occur as the following executions:

\[
\begin{align*}
po & \rightarrow contradicts \rightarrow co, \rightarrow rf, \rightarrow fr, \\
a: \ Wx=1 & \quad a: \ Rx=1 & \quad a: \ Wx=1 \\
b: \ Wx=2 & \quad b: \ Wx=1 & \quad rf \ b: \ Rx=0 \\
\end{align*}
\]

CoWW \hspace{2cm} CoRW1 \hspace{2cm} CoWR
Violations of coherence

There are five such cycles, which can occur as the following executions:

\[ \text{po} \rightarrow \text{co} \rightarrow \text{rf} \rightarrow \text{fr} \rightarrow \text{co} \rightarrow \text{rf} \rightarrow \]

\begin{align*}
\text{CoWW} & : \text{Wx}=1 \hspace{1cm} \text{a: Wx}=1 \hspace{1cm} \text{a: Wx}=1 \\
\text{CoRW1} & : \text{Rx}=1 \hspace{1cm} \text{b: Wx}=2 \hspace{1cm} \text{b: Wx}=1 \\
\text{CoWR} & : \text{Rx}=1 \hspace{1cm} \text{b: Wx}=1 \hspace{1cm} \text{rf} \hspace{1cm} \text{b: Rx}=0 \\
\text{CoRW2} & : \text{Rx}=2 \hspace{1cm} \text{c: Wx}=2 \\
\end{align*}
Violations of coherence

There are five such cycles, which can occur as the following executions:

\[ \text{po} \rightarrow \text{contradicts} \rightarrow \text{co, rf, fr, } \text{co, rf}, \text{fr}; \text{co, rf}; \text{fr}. \]

\begin{align*}
\text{CoWW} & : \begin{cases} a: W_x=1 \\ b: W_x=2 \end{cases} \\
\text{CoRW1} & : \begin{cases} a: R_x=1 \\ b: W_x=1 \end{cases} \\
\text{CoWR} & : \begin{cases} a: W_x=1 \\ b: R_x=0 \end{cases} \\
\text{CoRW2} & : \begin{cases} a: R_x=2 \\ c: W_x=2 \\ b: W_x=1 \end{cases} \\
\text{CoRR} & : \begin{cases} a: R_x=1 \\ c: W_x=1 \\ b: R_x=0 \end{cases}
\end{align*}
Building a test from a cycle

The conditions on locations and threads allows generating one test (program + final condition) from one cycle. Consider for instance:

\[ \text{fre} \rightarrow \text{rfe} \rightarrow \text{po} \rightarrow \text{rfe} \rightarrow \text{po} \]

- Set events (with directions, from communication relations)
Building a test from a cycle

The conditions on locations and threads allows generating one test (program + final condition) from one cycle. Consider for instance:

\[
\text{fre} \rightarrow \text{rfe} \rightarrow \text{po} \rightarrow \text{rfe} \rightarrow \text{po}
\]

- Set events (with directions, from communication relations)

\[
\text{fre} \rightarrow (a):W[?]? \rightarrow (b):R[?]? \rightarrow (c):W[?]? \rightarrow (d):R[?]? \rightarrow (e):W[?]?
\]
Building a test from a cycle

The conditions on locations and threads allows generating one test (program + final condition) from one cycle. Consider for instance:

\[
\text{fre} \rightarrow \text{rfe} \rightarrow \text{po} \rightarrow \text{rfe} \rightarrow \text{po}
\]

- Set events (with directions, from communication relations)

\[
\text{fre} \rightarrow (a):\text{W}[?]? \rightarrow (b):\text{R}[?]? \rightarrow (c):\text{W}[?]? \rightarrow (d):\text{R}[?]? \rightarrow (e):\text{W}[?]?
\]

- Set locations (one per \(\overset{\text{com}}{\rightarrow}\))

\[
\text{fre} \rightarrow (a):\text{W}[x]? \rightarrow (b):\text{R}[x]? \rightarrow (c):\text{W}[?]? \rightarrow (d):\text{R}[?]? \rightarrow (e):\text{R}[x]?
\]
Building a test from a cycle

The conditions on locations and threads allows generating one test (program + final condition) from one cycle. Consider for instance:

\[
\begin{align*}
\text{fre} & \rightarrow \text{rfe} \rightarrow \text{po} \rightarrow \text{rfe} \rightarrow \text{po} \\
\end{align*}
\]

- Set events (with directions, from communication relations)

\[
\begin{align*}
\text{fre} & \rightarrow (a):\text{W}[?]? \rightarrow (b):\text{R}[?]? \rightarrow (c):\text{W}[?]? \rightarrow (d):\text{R}[?]? \rightarrow (e):\text{W}[?]? \\
\end{align*}
\]

- Set locations (one per \(\text{com}\))

\[
\begin{align*}
\text{fre} & \rightarrow (a):\text{W}[x]? \rightarrow (b):\text{R}[x]? \rightarrow (c):\text{W}[y]? \rightarrow (d):\text{R}[y]? \rightarrow (e):\text{R}[x]? \\
\end{align*}
\]

- Set values for writes (initial value 0, then follow cycle: 1, 2, etc.)

\[
\begin{align*}
\text{fre} & \rightarrow (a):\text{W}[x]1 \rightarrow (b):\text{R}[x]? \rightarrow (c):\text{W}[y]1 \rightarrow (d):\text{R}[y]? \rightarrow (e):\text{R}[x]? \\
\end{align*}
\]
Building a test from a cycle

The conditions on locations and threads allows generating one test (program + final condition) from one cycle. Consider for instance:

\[ \text{fre} \rightarrow \text{rfe} \rightarrow \text{po} \rightarrow \text{rfe} \rightarrow \text{po} \]

- Set events (with directions, from communication relations)

\[ \text{fre} \rightarrow (a):W[?] \rightarrow \text{rfe} \rightarrow (b):R[?] \rightarrow \text{po} \rightarrow (c):W[?] \rightarrow \text{rfe} \rightarrow (d):R[?] \rightarrow \text{po} \rightarrow (e):W[?] \]

- Set locations (one per \(\overrightarrow{\text{com}}\))

\[ \text{fre} \rightarrow (a):W[x] \rightarrow \text{rfe} \rightarrow (b):R[x] \rightarrow \text{po} \rightarrow (c):W[y] \rightarrow \text{rfe} \rightarrow (d):R[y] \rightarrow \text{po} \rightarrow (e):R[x] \]

- Set values for writes (initial value 0, then follow cycle: 1, 2, etc.)

\[ \text{fre} \rightarrow (a):W[x]1 \rightarrow \text{rfe} \rightarrow (b):R[x] \rightarrow \text{po} \rightarrow (c):W[y]1 \rightarrow \text{rfe} \rightarrow (d):R[y] \rightarrow \text{po} \rightarrow (e):R[x] \]

- Set values for reads (consider \(\text{rfe} \rightarrow \text{R} \) or \(\text{R} \rightarrow \text{fre}\))

\[ \text{fre} \rightarrow (a):W[x]1 \rightarrow \text{rfe} \rightarrow (b):R[x]1 \rightarrow \text{po} \rightarrow (c):W[y]1 \rightarrow \text{rfe} \rightarrow (d):R[y]1 \rightarrow \text{po} \rightarrow (e):R[x]0 \]
Building a test from a cycle, continued

\[ \text{fre} \ (a): W[x]1 \xrightarrow{\text{rfe}} (b): R[x]1 \xrightarrow{\text{po}} (c): W[y]1 \xrightarrow{\text{rfe}} (d): R[y]1 \xrightarrow{\text{po}} (e): R[x]0 \]

- Build program from events (change thread at every $\xrightarrow{\text{com}}$).

<table>
<thead>
<tr>
<th></th>
<th>$T_0$</th>
<th>$T_1$</th>
<th>$T_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>$x \leftarrow 1$</td>
<td>(b)</td>
<td>$r0 \leftarrow x$</td>
</tr>
<tr>
<td>(c)</td>
<td>$y \leftarrow 1$</td>
<td>(e)</td>
<td>$r2 \leftarrow x$</td>
</tr>
</tbody>
</table>

- Build condition from coherence sequences (here nothing) and from values read.

Observed? $r0=1; r1=1; r2=0;$
Building another test, non-trivial coherence

Test $R$

\[
\begin{align*}
&\text{fre} \quad (a): W[x]1 \quad \text{po} \quad (b): W[y]1 \quad \text{coe} \quad (c): W[y]2 \quad \text{po} \quad (x): R[x]0
\end{align*}
\]

<table>
<thead>
<tr>
<th></th>
<th>$T_0$</th>
<th>$T_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(a)x \leftarrow 1$</td>
<td></td>
<td>$(c)y \leftarrow 2$</td>
</tr>
<tr>
<td>$(b)y \leftarrow 1$</td>
<td>$(d)r0 \leftarrow x$</td>
<td></td>
</tr>
</tbody>
</table>

Observed? $y=2$; $r0=0$

Here, coherence order is $0 \xrightarrow{\text{co}} 1 \xrightarrow{\text{co}} 2$, it suffices to read the final value.

Longer coherence orders command other techniques, for instance adding an observer thread.
A first tool: diyone

Generating **WRC**: 

```plaintext
% diyone -arch X86 Rfe Pod** Rfe Pod** Fre
X86 A
P0 | P1 | P2 ;
MOV [x],$1 | MOV EAX,[x] | MOV EAX,[y] ;
| MOV [y],$1 | MOV EBX,[x] ;
exists (1:EAX=1 /\ 2:EAX=1 /\ 2:EBX=0)
```

Doing the same for ARM is as simple as:

```plaintext
% diyone -arch ARM Rfe Pod** Rfe Pod** Fre
ARM A
{ %x0=x; %x1=x; %y1=y; %y2=y; %x2=x; }
P0 | P1 | P2 ;
MOV R0,#1 | LDR R0,[%x1] | LDR R0,[%y2] ;
| STR R0,[%x0] | MOV R1,#1 | LDR R1,[%x2] ;
                      | STR R1,[%y1] |
exists (1:R0=1 /\ 2:R0=1 /\ 2:R1=0)
```
Tool diyone, generating $\mathbb{R}$

% diyone -arch X86 PodWW Wse PodWR Fre
X86 A
"PodWW Wse PodWR Fre"
{ }
  P0 | P1 ;
  MOV [x],$1 | MOV [y],$2 ;
  MOV [y],$1 | MOV EAX,[x] ;
exists (y=2 \land 1:EAX=0)

Notice: We wrote PodWW, PodWR. The vocabulary of Candidate Relaxations is quite rich:

- Internal communications Rfi, Fri, Wsi.
- $\xrightarrow{\text{DO}}$ edges with identical target and source locations: PosRR, etc.
- Dependencies (DpAddrdW, etc.). fences (MFencedWR, etc.)
Application, testing non-SC executions for two threads

Cycle → execution → program + final condition.

All (critical) cycles for two threads: six cycles.

- **2+2W**: $po \rightarrow co \rightarrow po \rightarrow co$
- **LB**: $po \rightarrow rf \rightarrow po \rightarrow rf$
- **MP**: $po \rightarrow rf \rightarrow po \rightarrow fr$
- **R**: $po \rightarrow co \rightarrow po \rightarrow fr$
- **S**: $po \rightarrow rf \rightarrow po \rightarrow co$
- **SB**: $po \rightarrow fr \rightarrow po \rightarrow fr$

Save of coherence violation, any non-SC execution on two threads includes one of the above six cycles.

Hence, testing the six tests built from the six cycles gives reasonable coverage of possible SC violation on two threads. (Notice: coherence violations neglected).
Generating two-threads SC violations

The tool diy generates cycles (and tests) from a vocabulary of CR. It can be configured for the two threads case as follows:

-arch X86 # target architecture
-safe Pod**,Rfe,Fre,Wse # vocabulary
-nprocs 2 # 2 procs
-size 4 # max size of cycle (2 X nprocs)
-num false # for naming tests

Demo in demo/03.

% diy -conf 2.conf
Generator produced 6 tests
% ls
2+2W.litmus 2.conf @all LB.litmus
MP.litmus R.litmus SB.litmus S.litmus
% diy -conf 4.conf
Generator produced 68 tests...
Demo 03 continued, running the tests

Compiling:

% litmus -mach ./x86.cfg src/@all -o run
% make -C run -j 4

Running:

% cd run
% sh run.sh > X.00

Analysis:

% grep Observation X.00
Observation R Sometimes 79 1999921
Observation MP Never 0 2000000
Observation 2+2W Never 0 2000000
Observation S Never 0 2000000
Observation SB Sometimes 1194 1998806
Observation LB Never 0 2000000
Results for running the six tests on this machine

1. \(a: W_X=1\)  
   \(b: W_Y=1\)  
   \(c: W_Y=2\)  
   \(d: R_X=0\)  

2. \(a: W_X=2\)  
   \(b: W_Y=1\)  
   \(c: R_Y=1\)  
   \(d: W_X=1\)  

3. \(a: W_X=1\)  
   \(b: R_Y=0\)  
   \(c: W_Y=1\)  
   \(d: R_X=0\)  

4. \(a: W_X=1\)  
   \(b: W_Y=1\)  
   \(c: R_Y=1\)  
   \(d: R_X=0\)  

5. \(a: R_X=1\)  
   \(b: W_Y=1\)  
   \(c: R_Y=1\)  
   \(d: W_X=1\)  

6. \(a: W_X=2\)  
   \(b: W_Y=1\)  
   \(c: W_Y=2\)  
   \(d: W_X=1\)
Results for running the six tests on this machine

a: $W_x=1$  c: $W_y=2$

b: $W_y=1$  d: $R_x=0$

**R**: Ok

a: $W_x=2$  c: $R_y=1$

b: $W_y=1$  d: $W_x=1$

**S**: No

a: $W_x=1$  c: $R_y=1$

b: $W_y=1$  d: $R_x=0$

**MP**: No

a: $R_x=1$  c: $R_y=1$

b: $W_y=1$  d: $W_x=1$

**LB**: No

a: $W_x=2$  c: $W_y=2$

b: $W_y=1$  d: $W_x=1$

**SB**: Ok

2+2W: No
The write buffer explains how “reads can pass over writes”.
Axiomatic TSO

▸ Remember SC:

\[
\text{Acyclic} \left( \frac{\text{rf}}{\cup} \cup \frac{\text{co}}{\cup} \cup \frac{\text{fr}}{\cup} \cup \frac{\text{po}}{\cup} \right)
\]

A model for herd, our generic simulator:

let ppo = po \# ppo stands for ’preserved program-order’
let com-hb = fr \| rf \| co \# All communications create order
acyclic (ppo \| com-hb)

▸ In TSO:

▸ Write-to-read does not create order:

let ppo = RM(po) \| WW(po) \# WR(po) omitted

▸ Local reads do not create order:

let com-hb = rfe \| fr \| co \# rfi omitted

▸ TSO “happens-before” (HB) check:

acyclic (ppo \| com-hb \| mfence) as hb
Axiomatic TSO

- Remember SC:

\[
\text{Acyclic} \left( \frac{rf}{\rightarrow} \cup \frac{co}{\rightarrow} \cup \frac{fr}{\rightarrow} \cup \frac{po}{\rightarrow} \right)
\]

A model for herd, our generic simulator:

let ppo = po # ppo stands for 'preserved program-order'
let com-hb = fr | rf | co # All communications create order
acyclic (ppo | com-hb)

- In TSO:
  - Write-to-read does not create order:
    let ppo = RM(po) | WW(po) # WR(po) omitted
  - Local reads do not create order:
    let com-hb = rfe | fr | co # rfi omitted

- TSO "happens-before" (HB) check:
  acyclic (ppo | com-hb | mfence) as hb

Notice: Relations are between the points in time where a load binds its value and where a written value reaches memory.
Results for running the six test on the model

\[\begin{array}{cccc}
a: W_x=1 & c: W_y=2 & a: W_x=2 & c: R_y=1 \\
b: W_y=1 & d: R_x=0 & b: W_y=1 & d: W_x=1 \\
\end{array}\]

\[\begin{array}{cccc}
a: W_x=1 & c: R_y=1 & a: R_x=1 & c: R_y=1 \\
b: W_y=1 & d: R_x=0 & b: W_y=1 & d: W_x=1 \\
\end{array}\]

\[\begin{array}{cccc}
a: W_x=2 & c: W_y=2 & a: W_x=1 & c: W_y=1 \\
b: W_y=1 & d: W_x=1 & b: R_y=0 & d: R_x=0 \\
\end{array}\]
Results for running the six test on the model

a: $W_x=1$  c: $W_y=2$

b: $W_y=1$  d: $R_x=0$

R: Ok

48/74
Results for running the six tests on the model

<table>
<thead>
<tr>
<th>Test</th>
<th>Condition</th>
<th>Result</th>
<th>Condition</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Wx=1</td>
<td></td>
<td>b</td>
<td>Wy=1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>c</td>
<td>Wy=2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>d</td>
<td>Rx=0</td>
</tr>
<tr>
<td>R</td>
<td>Ok</td>
<td></td>
<td>S</td>
<td>No</td>
</tr>
</tbody>
</table>

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<td></td>
<td>b</td>
<td>Wy=1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>c</td>
<td>Ry=1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>d</td>
<td>Wx=1</td>
<td></td>
</tr>
</tbody>
</table>

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</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Rx=1</td>
<td></td>
<td>b</td>
<td>Wy=1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>c</td>
<td>Ry=1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>d</td>
<td>Wx=1</td>
<td></td>
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</tbody>
</table>

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<th>Condition</th>
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<th>Result</th>
</tr>
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<tr>
<td>a</td>
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<td></td>
<td>b</td>
<td>Wy=1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>c</td>
<td>Wy=2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>d</td>
<td>Wx=1</td>
<td></td>
</tr>
</tbody>
</table>

48/74
Results for running the six test on the model

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Wx</th>
<th>Wy</th>
<th>Rx</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Ok</td>
</tr>
<tr>
<td>b</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>No</td>
</tr>
<tr>
<td>c</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>Ok</td>
</tr>
<tr>
<td>d</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>No</td>
</tr>
</tbody>
</table>

R: Ok
S: No
SB: Ok

48/74
Results for running the six test on the model

a: \( Wx=1 \)  
b: \( Wy=1 \)  
c: \( Wy=2 \)  
d: \( Rx=0 \)

\( R: \text{Ok} \)

\( a: Wx=1 \)  
b: \( Wy=1 \)  
c: \( Ry=0 \)  
d: \( Rx=0 \)

\( MP: \text{No} \)

\( a: Wx=1 \)  
b: \( Wy=1 \)  
c: \( Ry=1 \)  
d: \( Rx=0 \)

\( S: \text{No} \)

\( a: Wx=2 \)  
b: \( Wy=1 \)  
c: \( Ry=1 \)  
d: \( Wx=1 \)

\( SB: \text{Ok} \)

\( a: Wx=1 \)  
b: \( Wy=1 \)  
c: \( Ry=1 \)  
d: \( Wx=1 \)

\( 2+2W: \text{No} \)
Internal \( \xrightarrow{\text{rf}} (\xrightarrow{\text{rfi}}) \) are not in HB

<table>
<thead>
<tr>
<th>SB+rfi-pos</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_0 )</td>
<td>(a) ( x \leftarrow 1 )</td>
<td>(c) ( r_1 \leftarrow y )</td>
</tr>
<tr>
<td>( T_1 )</td>
<td>(d) ( y \leftarrow 1 )</td>
<td>(f) ( r_3 \leftarrow x )</td>
</tr>
</tbody>
</table>

Observed? \( r_0=1; r_1=0; r_2=1; r_3=0; \)

- a: \( W_x=1 \)
- b: \( R_x=1 \)
- c: \( R_y=0 \)
- d: \( W_y=1 \)
- e: \( R_y=1 \)
- f: \( R_x=0 \)
Internal $\overset{rf}{\rightarrow} (\overset{rfi}{\rightarrow})$ are not in HB

<table>
<thead>
<tr>
<th>SB+rfi-pos</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_0$</td>
</tr>
<tr>
<td>(a) $x \leftarrow 1$</td>
</tr>
<tr>
<td>(b) $r0 \leftarrow x$</td>
</tr>
<tr>
<td>(c) $r1 \leftarrow y$</td>
</tr>
</tbody>
</table>

Observed? $r0=1; r1=0; r2=1; r3=0$;

a: $Wx=1$

b: $Rx=1$

c: $Ry=0$

d: $Wy=1$

e: $Ry=1$

SB+rfi-pos: Ok
Restoring SC

<table>
<thead>
<tr>
<th></th>
<th>$T_0$</th>
<th>$T_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(a)$</td>
<td>$x \leftarrow 1$</td>
<td>$(c)$</td>
</tr>
<tr>
<td>$(b)$</td>
<td>$y \leftarrow 1$</td>
<td>$(d)$</td>
</tr>
</tbody>
</table>

Observed? $y=2; \; r_0=0$

- a: $W_x=1$
- b: $W_y=1$
- c: $W_y=2$
- d: $R_x=0$
## Restoring SC with mfence

### Table: $R + \text{po} + \text{mfence}$

<table>
<thead>
<tr>
<th></th>
<th>$T_0$</th>
<th>$T_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>$x \leftarrow 1$</td>
<td>(c) $y \leftarrow 2$</td>
</tr>
<tr>
<td>(b)</td>
<td>$y \leftarrow 1$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(d) $r0 \leftarrow x$</td>
</tr>
</tbody>
</table>

**Observed?** $y=2; r0=0$

### Diagram:

```
  a: Wx=1  c: Wy=2
    po     mfence
  b: Wy=1  d: Rx=0
```

**Labels:**
- **po**
- **co**
- **fr**
- **mfence**
We are not done yet...

Our TSO model:

\[
\text{let ppo = RM(po) | WW(po) } # \text{ WR(po) omitted}
\]

\[
\text{let com-hb = rfe | fr | co } # \text{ rfi omitted}
\]

acyclic (ppo | com-hb)

show ppo | com-hb as hb

Allows two violations of coherence:

CoRW1

a: \( R_x = 1 \)  
\[ \text{po} \]  
\[ \text{rf} \]  
\[ b: \ W_x = 1 \]

CoWR

a: \( W_x = 1 \)  
\[ \text{fr} \]  
\[ \text{po} \]  
\[ rf \ b: \ R_x = 0 \]
We are not done yet...

Our TSO model:

\[
\text{let } ppo = \text{RM}(po) \mid \text{WW}(po) \quad \# \text{WR}(po) \text{ omitted} \\
\text{let } \text{com-hb} = \text{rfe} \mid \text{fr} \mid \text{co} \quad \# \text{rfi} \text{ omitted} \\
\text{acyclic (ppo } \mid \text{com-hb}) \\
\text{show } ppo \mid \text{com-hb as } \text{hb}
\]

Allows two violations of coherence:

\(\text{CoRW1}\)

\[
\begin{align*}
a: & \quad Rx=1 \\
b: & \quad Wx=1
\end{align*}
\]

\(\text{CoWR}\)

\[
\begin{align*}
a: & \quad Wx=1 \\
rf & \quad W \xrightarrow{po} R \text{ not in } \text{hb}
\end{align*}
\]

Those behaviours \textit{must} be rejected by our TSO model.
Correct axiomatic TSO

We add a specific UNIPROC check to rule out coherence violations:

\[
\text{Irreflexive} \left( \text{po-loc} \rightarrow; \hat{\text{com}} \rightarrow \right)
\]

Where \( \text{po-loc} \rightarrow \) is \( \text{po} \rightarrow \) between accesses to the same memory location.

irreflexive (po-loc; com+) as uniproc

... 

In the TSO case we can “optimise”:

irreflexive rf;RW(po-loc)
irreflexive fr;WR(po-loc)

because the other coherence violations are rejected by the HB check.
A word on **UNIPROC**

From cycle analysis, we have the attractive definition (since relying on local action of the core and on the existence of coherence orders):

**Definition (Uniproc 1)**

Program order $\text{po} \rightarrow$ does not contradict communication $\text{com}^+$. 

There is another definition “SC per location”. (Jason F. Cantin, Mikko H. Lipasti, James E. Smith ACM Symposium on Parallel Algorithms and Architectures 2004).

**Definition (Uniproc 2)**

Relation $\text{po-loc} \rightarrow \cup \text{com} \rightarrow$ is acyclic.

Definitions are equivalent.

It suffices to show that the existence of a cycle in $\text{po-loc} \rightarrow \cup \text{com} \rightarrow$ implies the existence of a coherence violation (*i.e.* a cycle $e_1 \rightarrow e_2 \rightarrow e_1$).
Consequence of $\xrightarrow{\text{co}}$ ordering writes

Lemma (Identical locations)

*Let* $e_1$, $e_2$ *be two different events with the same location,*

1. either $e_1 \xrightarrow{\text{com}} e_2$,
2. or $e_2 \xrightarrow{\text{com}} e_1$,
3. or $w \xrightarrow{\text{rf}} e_1$ and $w \xrightarrow{\text{rf}} e_2$.

Case analysis:

1. $w_1, w_2$, then either $w_1 \xrightarrow{\text{co}} w_2$ or $w_2 \xrightarrow{\text{co}} w_1$ (total order).
2. $r_1, r_2$, let $w_1 \xrightarrow{\text{rf}} r_1$ and $w_2 \xrightarrow{\text{rf}} r_2$. Then, either $w_1 = w_2$ and we are in case 3; or (for instance) $w_1 \xrightarrow{\text{co}} w_2$ and we have $r_1 \xrightarrow{\text{fr}} w_2 \xrightarrow{\text{rf}} r_2$.
3. $r_1, w_2$, let $w_1 \xrightarrow{\text{rf}} r_1$. Then, either $w_1 = w_2$ and $w_2 \xrightarrow{\text{rf}} r_1$; or $w_1 \xrightarrow{\text{co}} w_2$ and $r_1 \xrightarrow{\text{fr}} w_2$; or $w_2 \xrightarrow{\text{co}} w_1$ and $w_2 \xrightarrow{\text{co}} r_1$. 
Consequence of $\xrightarrow{\text{co}}$ ordering writes

**Lemma (Identical locations)**

Let $e_1$, $e_2$ be two different events with the same location,

1. either $e_1 \xrightarrow{\text{com}} e_2$,
2. or $e_2 \xrightarrow{\text{com}} e_1$,
3. or $w \xrightarrow{\text{rf}} e_1$ and $w \xrightarrow{\text{rf}} e_2$.

**Case analysis:**

- $w_1, w_2$, then either $w_1 \xrightarrow{\text{co}} w_2$ or $w_2 \xrightarrow{\text{co}} w_1$ (total order).
- $r_1, r_2$, let $w_1 \xrightarrow{\text{rf}} r_1$ and $w_2 \xrightarrow{\text{rf}} r_2$. Then, either $w_1 = w_2$ and we are in case 3; or (for instance) $w_1 \xrightarrow{\text{co}} w_2$ and we have $r_1 \xrightarrow{\text{fr}} w_2 \xrightarrow{\text{rf}} r_2$.
- $r_1, w_2$, let $w_1 \xrightarrow{\text{rf}} r_1$. Then, either $w_1 = w_2$ and $w_2 \xrightarrow{\text{rf}} r_1$; or $w_1 \xrightarrow{\text{co}} w_2$ and $r_1 \xrightarrow{\text{fr}} w_2$; or $w_2 \xrightarrow{\text{co}} w_1$ and $w_2 \xrightarrow{\text{co}} \xrightarrow{\text{rf}} r_1$.

**Corollary:** $\xrightarrow{\text{com}}$ is acyclic.
Equivalence of the two UNIPROC definitions

Proof is easy from “Identical locations” lemma.

Consider a cycle in $\xrightarrow{\text{pos}} \cup \xrightarrow{\text{com}}$.

- If there exists a $e_1 \xrightarrow{\text{po}} e_2$ step s.t. $e_2 \xrightarrow{\text{com}} e_1$, then we are done.
- Otherwise, for each $e_1 \xrightarrow{\text{po}} e_2$ step:
  - Either, $r_1 \xrightarrow{\text{po}} r_2$, with $w \xrightarrow{\text{rf}} r_1$ and $w \xrightarrow{\text{rf}} r_2$. We short-circuit the $\xrightarrow{\text{po}}$ step, replacing $w \xrightarrow{\text{rf}} r_1 \xrightarrow{\text{po}} r_2$ by $w \xrightarrow{\text{rf}} r_2$.
  - Or, $e_1 \xrightarrow{\text{com}} e_2$. We replace the $\xrightarrow{\text{po}}$ step by $\xrightarrow{\text{com}}$ steps.

As a result we have a cycle in $\xrightarrow{\text{com}}$, which is impossible.
A relaxed shared memory computer

More or less visible to user code:

- **Cores:**
  - Out of order execution
  - Branch speculation
  - Write buffers

- **Memory**
  - Physically distributed
  - Caches
Situation of (our) ARM/Power models

- **Architecture public reference** Informal, cannot clearly explain how fences restore SC for instance.

- **Simple, global-time model:** (CAV’10) too relaxed. It remains useful as it supports simple reasoning on SC-violations (CAV’11).

- **Operational model:** (PLDI’11) more precise, developed with IBM experts. It is quite complex, and the simulator is very slow.

- **Multi-event axiomatic model:** (CAV’12) more precise (equivalent to PLDI’11), uses several events per access.

- **Single-event axiomatic model:** (...) more precise (proved to be more relaxed than PLDI’11, experimentally equivalent). A more simple axiomatic model.

Joint work with (in order of appearance) Jade Alglave, Susmit Sarkar, Peter Sewell, Derek Williams, Kayvan Memarian, Scott Owens, Mark Batty, Sela Mador-Haim, Rajeev Alur, Milo M. K. Martin and Michael Tautschnig.
Some issues for ARM/Power

- No simple preserved-program-order. More precisely, $\xrightarrow{\text{ppo}}$ will now account for core constraints, such as dependencies.

- Communication relations alone do not define happen-before steps.

- A variety of memory fences: lightweight (Power lwsync) and full (Power sync).
Two-threads SC violation for ARM

Generating tests is as simple as:

% diy -conf 2.conf -arch ARM

With the same configuration file 2.conf as for X86.

Then, compile (in two steps, generate C locally, compile it on target machine), run and...

Observation R Sometimes 5722 1994278
Observation MP Sometimes 3571 1996429
Observation 2+2W Sometimes 17439 1982561
Observation S Sometimes 7270 1992730
Observation SB Sometimes 9788 1990212
Observation LB Sometimes 4782 1995218

All Non-SC behaviours observed!

No hope to define \( \rightarrow^{\text{ppo}} \) as simply as for TSO.
An experiment on ARM/Power

Consider test **MP**:  

<table>
<thead>
<tr>
<th></th>
<th>( T_0 )</th>
<th>( T_1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>( x \leftarrow 1 )</td>
<td>( r_0 \leftarrow y )</td>
</tr>
<tr>
<td>(b)</td>
<td>( y \leftarrow 1 )</td>
<td>( r_1 \leftarrow x )</td>
</tr>
</tbody>
</table>

Observed? \( r_0 = 1; \ r_1 = 0 \)

da: \( Wx = 1 \)   \( c: \) \( Ry = 1 \)
db: \( Wy = 1 \)   \( d: \) \( Rx = 0 \)

We know that the test is Ok (observed, valid) on ARM/Power, what does it take (amongst fences, dependencies,) to make the test No (unobserved, invalid)?

- **Fences**: \( \text{dsb}, \ \text{dmb}, \ \text{isb} \) (ARM); \( \text{sync}, \ \text{lwsync}, \ \text{isync} \) (Power).
- **Dependencies**: address, data, control, control+isb/isync.
Dependencies (Power)

Address dependency:

\[
\begin{align*}
    r1 & \leftarrow x \\
    r2 & \leftarrow t[r1]
\end{align*}
\]

\[
\begin{align*}
    \text{lwz } & r1,0(r8) \# r8 \text{ contains the address of } 'x' \\
    \text{slwi } & r7,r1,2 \# \text{sizeof(int)} = 4 \\
    \text{lwzx } & r2,r7,r9 \# r9 \text{ contains the address of } 't'
\end{align*}
\]

Data dependency:

\[
\begin{align*}
    r1 & \leftarrow x \\
    y & \leftarrow r1+1
\end{align*}
\]

\[
\begin{align*}
    \text{lwz } & r1,0(r8) \# r8 \text{ contains the address of } 'x' \\
    \text{addi } & r2,r1,1 \\
    \text{stw } & r2,0(r9) \# r9 \text{ contains the address of } 'y'
\end{align*}
\]

Control dependency:

\[
\begin{align*}
    r1 & \leftarrow x \\
    \text{if } r1=0 \text{ then}
\end{align*}
\]

\[
\begin{align*}
    y & \leftarrow 1 \\
    \text{li } & r2,1 \\
    \text{stw } & r2,0(r9)
\end{align*}
\]

L1:
Dependencies (Power)

Address dependency:

\[ r_1 \leftarrow x \]
\[ r_2 \leftarrow t[r_1] \]

\[
\begin{align*}
lwz & \quad r_1,0(r_8) \quad \text{# r8 contains the address of 'x'} \\
slwi & \quad r_7,r_1,2 \quad \text{# sizeof(int) = 4} \\
lwzx & \quad r_2,r_7,r_9 \quad \text{# r9 contains the address of 't'}
\end{align*}
\]

Data dependency:

\[ r_1 \leftarrow x \]
\[ y \leftarrow r_1 + 1 \]

\[
\begin{align*}
lwz & \quad r_1,0(r_8) \quad \text{# r8 contains the address of 'x'} \\
addi & \quad r_2,r_1,1 \\
stw & \quad r_2,0(r_9) \quad \text{# r9 contains the address of 'y'}
\end{align*}
\]

Control dependency: (+isync)

\[ r_1 \leftarrow x \]
\[ \text{if } r_1 = 0 \text{ then} \]
\[ (\text{isync}) \]
\[ y \leftarrow 1 \]

\[
\begin{align*}
lwz & \quad r_1,0(r_8) \\
cmpwi & \quad r_1,0 \\
bne & \quad L1 \\
li & \quad r_2,1 \\
stw & \quad r_2,0(r_9) \\
L1: & \quad \text{...}
\end{align*}
\]
Generating tests (ARM), yet another tool: diycross

Generating tests with diycross (demo in demo/04):

```
% diycross -arch ARM\nPodWW,DMBdWW,DSBdWW,ISBdWW\nRfe\nPodRR,DpCtrlldR,DpCtrlIsbdR,DpAddrdR,DMBdRR,DSBdRR,ISBdRR\nFre
Generator produced 28 tests
```

- One generates **MP** as diyone PodWW Rfe PodRR Fre
- diycross $r^1_{k_1}, \ldots, r^1_{N_1} \cdots r^M_{k_M}, \ldots, r^M_{N_M}$, generates the $N_1 \times \cdots \times N_M$ cycles $r^1_{k_1} \cdots r^\ell_{k_\ell} \cdots r^M_{k_M}$ by cross-producting the given CR list arguments.

This generates some variations in the **MP** family.

We then compile and run, and...
Optimal fencing/dependencies for MP
Optimal fencing for the 6 two-threads tests (Power)

- **R+syncs**
  - a: $W_x=1$
  - b: $W_y=1$
  - c: $W_y=2$
  - d: $R_x=0$

- **S+lwsync+addr**
  - a: $W_x=2$
  - b: $W_y=1$
  - c: $R_y=1$
  - d: $W_x=1$

- **SB+syncs**
  - a: $W_x=1$
  - b: $R_y=0$
  - c: $W_y=1$
  - d: $R_x=0$

- **MP+lwsync+addr**
  - a: $W_x=1$
  - b: $W_y=1$
  - c: $R_y=1$
  - d: $R_x=0$

- **LB+addrs**
  - a: $R_x=1$
  - b: $W_y=1$
  - c: $R_y=1$
  - d: $W_x=1$

- **2+2W+lwsyncs**
  - a: $W_x=2$
  - b: $W_y=1$
  - c: $W_y=2$
  - d: $W_x=1$
Some observations

In the previous slide we considered increasing power (and cost):

\[ \text{addr} < \text{lwsync} < \text{sync} \]

Then:

- Dependencies (address) are sufficient to restore order from reads to writes and reads in two-threads examples (but...)
- Fences restore order from writes to write and reads.
- Full fence (\text{sync}) is required from write to read.
- When to use the lightweight fence between writes is complex: \(2+2W+lwsyncs\) vs. \(R+syncs\).

![Diagram showing dependencies and fence usage]

\[\begin{align*}
  & a: Wx=2 \quad c: Wy=2 \\
  \text{lwsync} & \quad \text{lwsync} \\
  & b: Wy=1 \quad d: Wx=1
\end{align*}\]

\[\begin{align*}
  & a: Wx=1 \\
  \text{sync} & \quad \text{sync} \\
  & b: Wy=1 \quad d: Rx=0
\end{align*}\]

\(2+2W+lwsyncs\) vs. \(R+syncs\)

No \quad No
Some observations

In the previous slide we considered increasing power (and cost):

\[ \text{addr} < \text{lwsync} < \text{sync} \]

Then:

- Dependencies (address) are sufficient to restore order from reads to writes and reads in two-threads examples (but...)
- Fences restore order from writes to write and reads.
- Full fence (sync) is required from write to read.
- When to use the lightweight fence between writes is complex:
  \[ 2+2W+\text{lwsyncs} \text{ vs. } R+\text{lwsync}+\text{sync} \].

<table>
<thead>
<tr>
<th>Scenario</th>
<th>a</th>
<th>b</th>
<th>c</th>
<th>d</th>
</tr>
</thead>
<tbody>
<tr>
<td>lwsync</td>
<td></td>
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</tr>
<tr>
<td>lwsync</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R+lwsync+sync</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>a: Wx=1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>b: Wy=1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>c: Wy=2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>d: Rx=0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\[ 2+2W+\text{lwsyncs} \]

No

\[ R+\text{lwsync}+\text{sync} \]

Ok
Dependencies are enough

<table>
<thead>
<tr>
<th>LB+datas</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_0$</td>
</tr>
<tr>
<td>(a) $r_0 \leftarrow x$</td>
</tr>
<tr>
<td>(b) $y \leftarrow r_0$</td>
</tr>
</tbody>
</table>

Observed? $r_0=42$; $r_1=42$;

- a: $Rx=42$
- b: $Wy=42$
- c: $Ry=42$
- d: $Wx=42$

Of course we never observe this behaviour (values out of thin air) and any (hardware) model should forbid it.

**Happens-before** If we order: (1) stores: the point in time when the value is made available to other threads (2) loads: the point when the value is read by core.
Dependencies from reads not always enough!

Consider test \textbf{WRC+data+addr}:

<table>
<thead>
<tr>
<th></th>
<th>$T_0$</th>
<th>$T_1$</th>
<th>$T_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>$x \leftarrow 1$</td>
<td>(b) $r_0 \leftarrow x$</td>
<td>(d) $r_1 \leftarrow y$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(c) $y \leftarrow 1$</td>
<td>(e) $r_2 \leftarrow x$</td>
</tr>
<tr>
<td>Observed?</td>
<td>$r_0=1$; $r_1=1$; $r_2=0$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **a**: $W_x=1$  
- **b**: $R_x=1$
- **d**: $R_y=1$
- **c**: $W_y=1$
- **e**: $R_x=0$

Behaviour observed on Power 6 and 7 (not on ARM, but documentation allows it).

**Stores are not “multi-copy atomic”** $T_0$ and $T_1$ share a private buffer/cache/memory (e.g. a cache in SMT context). $T_2$ “does not see” the store by $T_0$, when $T_1$ does.
Restoring SC for **WRC**

Use a lightweight fence on $T_1$:

\[
\begin{align*}
T_0 & \quad T_1 & \quad T_2 \\
a: \ Wx=1 & \quad b: \ Rx=1 & \quad d: \ Ry=1 \\
c: \ Wy=1 & \quad e: \ Rx=0
\end{align*}
\]

WRC+lwsync+addr

**Observation:** The fence orders the writes $a$ (by $T_0$) and $c$ (by $T_1$) for any observer (here $T_2$).
Another case of unsufficient dependencies

Consider test **IRIW+addr**: 

<table>
<thead>
<tr>
<th></th>
<th>(T_0)</th>
<th>(T_1)</th>
<th>(T_2)</th>
<th>(T_3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>(x \leftarrow 1)</td>
<td>(b)</td>
<td>(r_0 \leftarrow x)</td>
<td>(d)</td>
</tr>
<tr>
<td>(c)</td>
<td>(r_1 \leftarrow y)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Observed? \(r_0=1; r_1=0; r_2=1; r_3=0;\)

- \(a\): \(W_x=1\)
- \(b\): \(R_x=1\)
- \(d\): \(W_y=1\)
- \(e\): \(R_y=1\)
- \(c\): \(R_y=0\)
- \(f\): \(R_x=0\)

Behaviour observed on Power (not on ARM, but documentation allows it).

**Stores are not “multi-copy atomic”**: \(T_0\) and \(T_1\) have a private buffer/cache/memory, \(T_2\) and \(T_3\) also have one.
Restoring SC for IRIW

Use a full fence on $T_1$ and $T_2$:

- $T_0$: $Wx=1$
- $T_1$: $Rx=1$
- $T_2$: $Wy=1$
- $T_3$: $Rx=0$
- $T_0$: $Ry=0$
- $T_1$: $Wy=1$
- $T_2$: $Ry=1$
- $T_3$: $Rx=0$

**Propagation:** Full fences order all communications.
Relation summary

Communication relations:
- **Read-from:** $w \xrightarrow{\text{rf}} r$, with $\text{loc}(w) = \text{loc}(r), \text{val}(w) = \text{val}(r)$.
- **Coherence:** $w \xrightarrow{\text{co}} w'$, with $\text{loc}(w) = \text{loc}(w') = x$. Total order for given $x$: hence “coherence orders”.
- We deduce from-read: $r \xrightarrow{\text{fr}} w$, i.e $w' \xrightarrow{\text{rf}} r$ and $w' \xrightarrow{\text{co}} w$.
- We distinguish internal (same proc, $\xrightarrow{\text{rfi}}, \xrightarrow{\text{coi}}, \xrightarrow{\text{fri}}$) and external (different procs, $\xrightarrow{\text{rfe}}, \xrightarrow{\text{coe}}, \xrightarrow{\text{fre}}$) communications.

“Execution” relations
- **Program order:** $e_1 \xrightarrow{\text{po}} e_2$, with $\text{proc}(e_1) = \text{proc}(e_2)$.
- **Same location program order:** $e_1 \xrightarrow{\text{po-loc}} e_2$.
- **Preserved program order:** $e_1 \xrightarrow{\text{ppo}} e_2$, with $\xrightarrow{\text{ppo}} \subseteq \xrightarrow{\text{po}}$. Computed from other relations.
- **Fences:** effective strong and lightweight fences in between events $\xrightarrow{\text{strong}}$ and $\xrightarrow{\text{light}}$. Effective means that for instance $w \xrightarrow{\text{lwsync}} r$ does not implies $w \xrightarrow{\text{light}} r$. 
A model in four checks

UNIPROC

acyclic poloc | com as uniproc

HB

let fence = strong | light
let hb = ppo | fence | rfe
acyclic hb

OBSERVATION  We now define the effect of fences (any fence) for ordering writes:

let propbase = (WW(fence)| (rfe;RW(fence)));hb*
irreflexive fre;propbase as observation

PROPAGATION  Strong fences wait for all communications.

let propstrong = com*; propbase*; strong; hb*
let prop = WW(propbase)| (com*;propbase*;strong;hb*)
acyclic co | prop as propagation
ARM/Power preserved program order

Rather complex, results from a two events per access analysis (cf. CAV’12).

(* Utilities *)
let dd = addr | data
let rdw = po-loc & (fre;rfe)
let detour = po-loc & (coe ; rfe)
let addrpo = addr;po

(* Initial value *)
let ci0 = ctrlisync | detour
let ii0 = dd | rfi | rdw
let cc0 = dd | po-loc | ctrl | addrpo
let ic0 = 0

(* Fixpoint from i -> c in instructions and transitivity *)
let rec ci = ci0 | (ci;ii) | (cc;ci)
and ii = ii0 | ci | (ic;ci) | (ii;ii)
and cc = cc0 | ci | (ci;ic) | (cc;cc)
and ic = ic0 | ii | cc | (ic;cc) | (ii ; ic)

let ppo = RW(ic) | RR(ii)

Can be limited to dependencies...
How good is our model?

Is it sound?

▶ A proof: any behaviour allowed is also allowed by the operational model of PLDI’11.
▶ Experiments
  ▶ Soundness w.r.t. hardware (ARM being a bit problematic because of acknowledged read-after-read hazard).
  ▶ Experimental equivalence with our previous models, saved from current debate on some subtle semantical point for lwsync.

In any case:

▶ Simulation is fast (\(\times 1000\) w.r.t. PLDI’11) (\(\times 10\) w.r.t. CAV’12).
▶ The existence of four checks UNIPROC, HB OBSERVATION and PROPAGATION stand on firm bases.
▶ The semantics of strong fences also does.
▶ The model and simulator (i.e. herd) are flexible, one easily change a few relations (e.g. \(\overrightarrow{p^p}\), or the semantics of weak fences).
Subtle point

<table>
<thead>
<tr>
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<th>$T_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>$x \leftarrow 2$</td>
<td>(c) $y \leftarrow 2$</td>
<td>(d) $r_0 \leftarrow z$</td>
</tr>
<tr>
<td>(d)</td>
<td>$y \leftarrow 1$</td>
<td>(e) $z \leftarrow 1$</td>
<td>(f) $x \leftarrow 1$</td>
</tr>
</tbody>
</table>

Observed? $x=2; y=2; r_0=1$

Unobserved and forbidden by model. May be allowed...
A test of coherence violation

Our setting also finds bugs... The following execution:

is observed on all (tested) ARM machines. It features a CoRR-style coherence violation (i.e. $\text{po} \rightarrow$ contradicts $\text{fr} \rightarrow$; $\text{fr} \rightarrow$).